


**INFORMATION DISCLOSURE STATEMENT  
BY APPLICANT**

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First Named Inventor	Cheng
Art Unit	2133
Examiner Name	

Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
PC		Bhavsar, "An Algorithm for Row-Column Self-Repair of RAMs and Its Implementation in the Alpha 21264", <i>Proc. IEEE Int'l Test Conference</i> , pp. 311-318 (1999).
PC		Haddad et al., "Increased Throughput for the Testing and Repair of RAM's with Redundancy," <i>IEEE Transactions on Computers</i> , Vol. 40, No. 2, pp. 154-166 (February 1991).
PC		Horstmann et al., "Metastability Behavior of CMOS ASIC Flip-Flops in Theory and Test," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 24, No. 1, pp. 146-157 (February 1989).
PC		Kawagoe et al., "A Built-in Self-repair Analyzer (CRESTA) for Embedded DRAMs", <i>Proc. IEEE Int'l Test Conference</i> , pp. 567-574 (2000).
PC		Kim et al., "Built In Self Repair for Embedded High Density SRAM", <i>Proc. IEEE Int'l Test Conference</i> , pp. 1112-1119 (1998).
PC		Nakahara et al., "Built in Self-test for GHz Embedded SRAMs Using Flexible Pattern Generator and New Repair Algorithm", <i>Proc. IEEE Int'l Test Conference</i> , pp 301-310 (1999).
PC		Powell et al., "BIST for Deep Submicron ASIC Memories with High Performance Application", <i>ITC 2003 (to appear)</i>
PC		Shoukourian et al., "An Approach for Evaluation of Redundancy Analysis Algorithms", <i>Proc. IEEE MTDT Workshop</i> , San Jose, pp. 51-55, 2001
PC		Venkatesh et al., "A Fault Modeling Technique to Test Memory BIST Algorithms", <i>Memory Technology, Design and Testing</i> , <i>Proc. of the 2002 IEEE Int'l Workshop</i> , pp. 109-116 (2002).
PC		Zorian, "Embedded Memory Test & Repair: Infrastructure IP for SOC Yield", <i>Proc. IEEE Int'l Test Conference</i> , pp. 340-349 (2002).

EXAMINER SIGNATURE:	/Phung Chung/	DATE CONSIDERED:	05/18/2006
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\* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.